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10/695,779	10/30/2003	Joseph P. Kennedy	1163.00	6911

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EXAMINER	
MOON, SEOKYUN	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,779	KENNEDY ET AL.	
	Examiner	Art Unit	
	SEOKYUN MOON	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 11-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,11-17 and 19-31* is/are rejected.

7)☒ Claim(s) *18 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The Applicant's arguments filed on December 10, 2007 have been fully considered.

The Applicant pointed out that the cited prior art (US 6,337,682, herein after "*Hwang*") does not teach the claim limitation, "*wherein the reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a convergence time, wherein the duration of the convergence time is programmable*" [Applicant's Remark: pg 12 and pg 14].

Examiner respectfully disagrees.

On col. 5 lines 18-21, Hwang discloses the micro-controller generating a frequency divisional value corresponding to the present display mode. In other words, in the device of Hwang, the frequency divisional values for respective display mode are programmed in the micro-controller. Thus, in the device of Hwang, the frequency divisional value is programmable. As shown on figs 1 and 2, Hwang teaches a phase lock loop synchronizing the clock signal CLK1 with the horizontal synchronous signal, and as shown on fig. 2, the locking rate of the phase lock loop is determined by the frequency divisional value. Since the locking rate of the phase lock loop is inversely proportional to the locking period of the phase lock loop, the locking period is programmable. Furthermore, since the locking period represents the time period used to lock/synchronize/converge the clock signal with the horizontal synchronous signal, Hwang does teach the duration of the convergence time being programmable.

Accordingly, the Examiner respectfully submits that the Applicant's arguments regarding the claim limitation are not persuasive.

Furthermore, since the locking period is the period between the beginning of the locking process and the ending of the locking process, the Examiner respectfully submits that Hwang does teach the

newly added claim limitation, "*said duration of the convergence time beginning at the start of convergence and ending at the achievement of convergence*", as well.

Remark

2. Claims 11-13 and 15-18 were indicated as being allowable.

However, in this correspondence, claims 11-13 and 15-17 are rejected.

Accordingly, this Office Action is made Non-Final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1**, **11**, **14**, **21-23**, and **27-28** are rejected under 35 U.S.C. 102(b) as being anticipated by Hwang (US 6,337,682).

As to **claim 1**, Hwang teaches an image display system for synchronizing the display of images on a plurality of display devices (the display panel of "*the flat panel display apparatus*" and the display of the "*personal computer system*") [col. 1 lines 21-23], comprising:

a first computer system ("*personal computer system*") [col. 1 lines 21-23] generating a first signal ("*analog video signal*") representing first image data to be displayed on a first display device;

a second computer system ("*the flat panel display apparatus*") [col. 1 lines 21-25] generating a second signal ("*digital video signal*") representing second image data to be displayed on a second display device; and

means for synchronizing the first and second image data [fig. 3], the synchronizing means comprising:

a master sync signal generator generating a master sync signal (the means for generating "*Hsync*"), and

a signal generating means (a combination of "*preamplifier 10*", "*ADC 20*", "*delay circuit 50*", "*micro-controller 60*" and "*PLL 40*") for receiving the master sync signal and generating a video clock signal ("*CLK 1*") from the master sync signal wherein the video clock signal is synchronized with the master sync signal;

a comparison means (a combination of "*phase detector 70*" and "*comparator 65*") for determining if the video clock signal is no longer synchronized with the master sync signal [col. 5 lines 41-44];

wherein in response to the comparison means determining that the video clock signal is no longer synchronized with the master sync signal, the signal generating means reestablishes the synchronization between the video clock signal and the master sync signal [col. 6 lines 27-38]; and

wherein the reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a convergence time, wherein the duration of the convergence time is programmable, the duration of the convergence time beginning at the start of convergence and ending at the achievement of convergence (as discussed in "*Response to Arguments*" section).

As to **claim 11**, Hwang teaches an apparatus [figs. 2 and 3] for synchronizing to a first digital signal ("*Hsync* ") [fig. 2], generation of a second digital signal ("*CLK1*") [fig. 2], comprising:

a phase detector ("*phase detector 41*") for comparing the first digital signal to a comparison pulse stream (the output of the "*frequency divider 44*") to produce a difference pulse stream (the output of the "*phase detector 41*");

a low pass filter ("*LPF* 42") for filtering the difference pulse stream to produce an analog signal (the output of the "*LPF 42*");

a voltage controlled oscillator ("*VCO 43*") for producing the second digital signal in response to the analog signal;

and a digital rate controller (a combination of "*micro-controller 60*" and "*frequency divider 44*") that divides the second digital signal ("*CLK 1*") by a divisor value ("*f.d.v.*") to produce the comparison pulse stream, wherein the digital rate controller produces the divisor value based on a programmable rate value ("*f.d.v.*") (note that since the frequency divisional value determines the locking rate of the phase locked loop, the frequency divisional value is a rate value, and since the frequency divisional value has different value depending on the present display mode, the frequency divisional value is programmed differently depending on various display modes. Thus, the frequency divisional value is a programmable rate value) and a comparison of the first digital signal and the comparison pulse stream (based on the output of "*VCO 43*", which is determined based on a comparison of "*Hsync*" and the output of the "*frequency divider 44*").

As to **claim 14**, Hwang [figs. 2 and 3] teaches that the signal generating means comprises a video input/output module comprised of a phase locked loop circuit (a combination of "*phase detector 41*", "*LPF 42*", and "*VCO 43*") and a programmable digital rate controller (a combination of "*frequency divider 44*" and "*micro-controller 60*");

wherein the phase-locked loop circuit ("*PLL 40*") generates the video clock signal ("*CLK 1*");

wherein the phase-locked loop circuit reestablishes the synchronization between the video clock signal and the master sync signal [col. 6 lines 27-38];

wherein the programmable digital rate controller determines if the video clock signal is no longer synchronized with the master sync signal [col. 5 lines 41-44]; and

wherein the programmable digital rate controller further controls a lock responsiveness rate at which the phase-locked loop circuit reestablishes the synchronization between the video clock signal and the master sync signal (by adjusting the frequency divisional value, the frequency of the sampling clock

signal CLK1 is adjusted), wherein a faster lock responsiveness rate results in a shorter convergence time and a slower lock responsiveness rate results in a longer convergence time (as the frequency divisional value is adjusted, the lock responsiveness rate increases/decreases and thus results in that the locking occurs within a shorter / a longer time period).

As to **claim 21**, Hwang inherently teaches each of the first image data and the second image data comprising a respective computer graphic image since each of the display panel of Hwang's computer and the display panel of Hwang's flat panel display apparatus displays computer graphic images.

As to **claim 22**, Hwang inherently teaches each of the first and second computer systems further comprising a respective graphic processor for generating the respective computer graphics image since it is required for Hwang's computer and the flat panel display to include graphic processors to generate images on the display panels.

As to **claim 23**, Hwang teaches each graphics processor generating the computer graphics image in response to the video clock signal which is synchronized to the master sync signal [col. 5 line 65 – col. 6 line 2].

As to **claim 27**, all of the claim limitations have already been discussed with respect to the rejection of claim 1 except for a speed of the convergence of the video clock signal and the master sync signal being programmably adjustable.

Hwang teaches the speed of the convergence of the video clock signal and the master sync signal being programmably adjustable [col. 5 lines 30-39 and col. 5 lines 18-21].

As to **claim 28**, all of the claim limitations have already been discussed with respect to the rejection of claim 14.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 12**, **13**, **15-17**, **19**, **20**, **24-26**, and **29-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang.

As to **claim 12**, Hwang teaches a system for synchronizing video frame rate between a first video system displaying video images on a first display device and a second video system displaying video images on a second display device, the system comprising:

a master sync signal generator (means for generating "*Hsync*") [fig. 3];

and a video input/output module associated with the second video system,

wherein the video input/output module comprises a sync separator (means included in the "*Micro-controller 60*") [fig. 3] that receives the master sync signal ("*Hsync*") [fig. 3] and produces a master pulse stream ("*Hsync* ") therefrom;

a phase detector ("*phase detector 41*") [fig. 2] that compares the master pulse stream to a slave pulse stream to produce a difference pulse stream (the output from the "*phase detector 41*");

a low pass filter ("*LPF 42*") that filters the different pulse stream to produce an analog signal;

a voltage controlled oscillator ("*VCO 43*") that produces a video clock signal in response to the analog signal;

and a digital rate controller (a combination of "*frequency divider 44*" and means for determining/outputting "*f.d.v.*") [fig. 2] that divides the clock signal ("*CLK1*") by a divisor value to produce the slave pulse stream, the digital rate controller producing the divisor value based on a programmable rate value and a comparison of the master pulse stream and the slave pulse stream (as discussed in "*Response to Arguments*" section).

Hwang does not expressly disclose the first computer system comprising the input/output module processing the image data.

However, the courts have held that a mere duplication of the components of the device is generally recognized as being within the level of ordinary skill in the art. *St Regis Paper Co. v. Bemis Co. Inc. 193 USPQ 8, 11 (7 TM Cir. 1977).*

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the input/output module in the display of the first computer system, in order to allow the display of the first computer system to be synchronized to other displays.

As to **claim 13**, Hwang teaches the video input/output modules further comprising a video generator ("*ADC 20*") [fig. 3] generating a video signal in response to the clock signal.

As to **claim 15**, Hwang teaches that the video input/output module (a combination of "*micro-controller 60*" and "*PLL 40*") [fig. 3] comprising the programmable digital rate controller (a combination of "*frequency divider 44*" and "*micro-controller 60*") for receiving the master sync signal ("*Hsync*") and extracting a master pulse stream ("*Hsync* ") from the master sync signal.

Hwang does not expressly teach the video input/output module comprising a separated device, a sync separator, for receiving the master sync signal and extracting a master pulse stream from the master sync signal. (i.e., in the device of Hwang, the programmable digital rate controller controls the lock responsiveness rate and extracts a master pulse stream from the master sync signal).

However, the courts have held that separating a single part ("*micro-controller 60*") into a plurality of separated parts (the programmable digital rate controller and a sync separator) is generally recognized as being within the level of ordinary skill in the art. *In re Dulberg*, 289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the image display system of Hwang to include a sync separator and a programmable digital rate controller, separately, in order to allow to implement each of the sync separator and the programmable digital rate controller separately, and thus to allow to replace each of the components,

easily.

As to **claim 16**, Hwang teaches the phase-locked loop circuit (a combination of "*phase detector 41*", "*LPF 42*", and "*VCO 43*") [fig. 2] being comprised of:

a phase detector ("*phase detector 41*") for comparing the received master pulse stream ("*Hsync*") to a received slave pulse stream (the output of the "*frequency divider 44*") to produce a difference pulse stream (the output of the "*phase detector 41*"), wherein the width of a difference pulse in the difference pulse stream represents a difference between the master pulse stream and the slave pulse stream;

a low pass filter ("*LPF 42*") for filtering the difference pulse stream to produce an analog signal; and

a voltage controlled oscillator ("*VCO 43*") for generating the video clock signal in response to the analog signal.

As to **claim 17**, Hwang teaches the programmable digital rate controller (a combination of "*frequency divider 44*" and "*micro-controller 60*") [fig. 2] receiving the video clock signal ("*CLK1*");

wherein the programmable digital rate controller divides the video clock signal by a divisor value to produce the slave pulse stream (the output of the "*frequency divider 44*"); and

wherein the programmable digital rate controller generates the divisor value ("*f.d.v.*") based on a programmable lock speed and a comparison of the master pulse stream and the slave pulse stream.

As to **claim 19**, Hwang teaches the second computer system comprising the input/output module processing the image data.

Hwang does not expressly disclose the first computer system comprising the input/output module processing the image data.

However, the courts have held that a mere duplication of the components of the device is generally recognized as being within the level of ordinary skill in the art. *St Regis Paper Co. v. Bemis Co. Inc. 193 USPQ 8, 11 (7 TM Cir. 1977).*

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the input/output module in the display of the first computer system, in order to allow the display of the first computer system to be synchronized to other displays.

As to **claim 20**, Hwang [fig. 3] teaches the video input/output module comprising a video generator ("*ADC 20*") for generating a video signal in response to the video clock signal ("*CLK 1*") which is synchronized to the master sync signal.

As to **claim 24**, Hwang teaches the signal generating means comprising a video input/output module, the first computer system comprising a video input/output module, and the second computer system comprising a video input/output modules which receives master sync signal from the master sync signal generator, as discussed with respect to the rejection of claims 19 and 25.

Hwang does not expressly disclose the master sync signal generator being external to the first computer system and the video input/output module of the first computer to receive the master sync signal.

However, as Examiner acknowledges that specifying the master sync signal generator being external to the first computer system and the video input/output module of the first computer system receiving the master sync signal from the master sync signal generator, is not a required design layout/specification but is one of a plurality of design layouts, which includes a design layout described in claim 25, it is an obvious matter of design choice to have such an arrangement of the computer systems and to specify the master sync signal generator being external to the first and the second computer systems.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the image display system of Hwang to specify the master sync signal generator being external to the first and the second computer system since any one of the design layouts/options, i.e. including the master sync signal generator in the first computer system or placing the master sync signal

generator external to the first and the second computer systems would perform equally well at synchronizing the video clock signal outputted from the second computer system to the master sync signal.

As to **claim 25**, Hwang teaches the image display system,

wherein the signal generating means comprises a video input/output module [fig. 3];

wherein the first computer system ("*personal computer system*") comprises the master sync signal ("*Hsync*") generator [col. 1 lines 21-25];

wherein the second computer system comprises the video input/output module [fig. 3]; and

wherein the video input/output module synchronizes to the master sync signal ("*Hsync*") received from the master sync signal generator;

wherein the first computer system is a master computer system and the second computer system is a slave display system [col. 1 lines 21-25].

As to **claim 26**, Hwang teaches the master sync signal being generated from a graphic processor of the master computer system [col. 1 lines 21-25].

As to **claim 29**, all of the claim limitations have already been discussed with respect to the rejection of claim 15.

As to **claim 30**, all of the claim limitations have already been discussed with respect to the rejection of claim 16.

As to **claim 31**, all of the claim limitations have already been discussed with respect to the rejection of claim 17.

Allowable Subject Matter

7. **Claims 18** and **32** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEOKYUN MOON whose telephone number is (571)272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 17, 2008
/Seokyun Moon/
Examiner, Art Unit 2629

/Alexander Eisen/

Supervisory Patent Examiner, Art Unit 2629